

# Homework #1

**Problem #1 (5 pts.)**

Given a generic combinational block with 4 inputs a 1 output, how many different logic functions can you build? Explain why.

**Problem #2 (45 pts.)**

Design a 3 bit binary counter. Assume that the only cells available are D-Flip flops and 2-input NAND gates. The NAND gates have a TYP. delay of 1ns. The flip-flops have a TYP. D-to-Q delay of 1 ns, setup time of 0.1 ns and hold time of 0.08 ns. (Assume a derating factor of 2 between WORST and TYP. and between TYP. and BEST).

1. Draw the gate level schematic of the counter
2. Find out what is the max frequency (min clock period) for which you can use the counter you designed
3. Assume a clock cycle of T=10 ns, and check if setup and hold time constraints are respected.

**Problem #3 (20 pts.)**

Using only a D-flip flop and any number and kind of logic gates you like design a circuit that implements the following functionality:

Inputs		Output
A	B	$Q_{n+1}$
0	0	not( $Q_n$ )
0	1	1
1	0	0
1	1	$Q_n$

**Problem #4 (30 pts.)**

Design a state machine (up to gate level) able to perform edge detection. Each time your data input signal “DI” has an edge, at the next closest positive clock edge, you have to generate a pulse that last exactly one clock cycle. If the asynchronous reset input (RST) is asserted the output “DO” must be set to logic 0. (See the waveform example)

